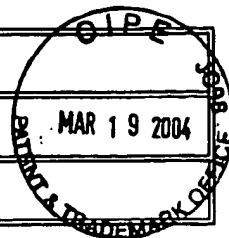


<b>INFORMATION DISCLOSURE CITATION PTO-1449</b>	Atty. Docket No. 970607B	Serial No. 10/050,169
	Applicant(s): Shinichiroh IKEMASU et al.	
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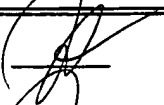
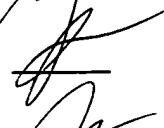



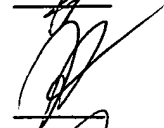
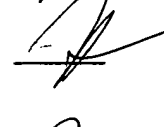



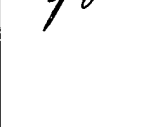
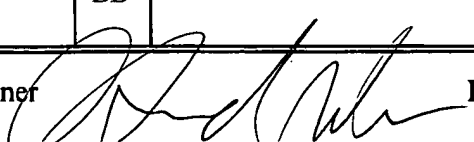


### U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
	AA	5,605,857	Jost et al.			02/97
	AB	5,324,681	Lowrey et al.			06/94
	AC	5,292,677	Dennison			03/94
	AD	5,281,549	Fazan et al.			01/94
	AE	5,760,429	Yano et al.			6/98
	AF	5,479,054	Tottori			12/95
	AG	5,150,278 <sup>6</sup>	Gonzalez et al.			9/92
	AH					
	AI					
	AJ					
	AK					
	AL					
	AM					
	AN					
	AO					



## OTHER DOCUMENTS

	AP	B.LUTHER et al.; Planar Copper-Polyimide Back End of the Line"; Proceedings of 10 <sup>th</sup> International VMIC; pages 15-21; June 1993.
	AQ	B.M. SOMERO et al.; "A Modular in-situ Integration Scheme for Deep Submicron", Proceedings of 10 <sup>th</sup> International VMIC; pages 28-34; June 1993.
	AR	M.F. CHISHOLM et al.; "A High Performance 0.5 um Five-Level Metal Process with Extendibility of Sub-Half Micron"; pages 22-28; June 1994.
	AS	M. RUTTEN et al.; "Pattern Density Effects in Tungsten CMP", Proceedings of 12 <sup>th</sup> International VMIC; pages 491-497; June 1995.
	AT	I. NAIKI et al.; "Center Wordline Cell: A New Symmetric Layout Cell for 64Mb SRAM"; Technical Digest of IEDM; pages 817-820; December 1993.
	AU	T. KAGA et al.; "A 0.29-um <sup>2</sup> MIM-Crown Cell and Process Technologies for 1-Gigabit DRAMs"; Technical Digest of IEDM; pages 927-929; December 1994.
	AV	H.K. KANG et al.; "Highly Manufacturable Process Technology for Reliable 256 Mbit and 1 Gbit DRAMs"; Technical Digest of IEDM; pages 635-638; December 1994.
	A W	Y. OHJI et al.; "Ta <sub>2</sub> O <sub>5</sub> Capacitors Dielectric Material for Giga-bit DRAMs"; Technical Digest of IEDM; pages 111-114; December 1995.
	A X	Y. NISHIOKA et al.; "Giga-bit Scale DRAM Cell with New Simple Ru/(Ba,Sr)TiO <sub>3</sub> /Ru Stacked Capacitors Using X-ray Lithography"; Technical Digest of IEDM; pages 903-906; December 1995.
	AY	K.P. LEE et al.; "A Process Technology for 1 Giga-bit DRAM"; Technical Digest of IEDM; pages 907-910; December 1995.
	AZ	J.K. PARK et al.; "Isolation Merged Bit Line Cell(IMBC) for 1Gb DRAM and Beyond". Technical Digest of IEDM; pages 911-914; December 1995.
_____	B A	
_____	BB	
Examiner 	Date Considered	6/17/04